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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/874,458	06/04/2001	James G. Judkins	110604BGA.US	5819

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EXAMINER

LUU, PHO M

ART UNIT	PAPER NUMBER
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2824

DATE MAILED: 12/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

9/m

Office Action Summary

Application No.

09/874,458

Applicant(s)

JUDKINS, JAMES G.

Examiner

Pho M Luu

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 10-21 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4-6 and 8 is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☒ Claim(s) 7 and 9 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 June 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). ____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ 6) ☒ Other: *Search History*

DETAILED ACTION

Election/Restrictions

1. Claims 10-21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election of Group I, claims 1-9, was made without traverse in Paper No 3.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 4, node **84**.

3. The drawings are objected to because the resistor connected to the voltage source **VSS** does not have a reference number nor is mentioned in the Specification.

Correction is required.

4. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

5. The abstract of the disclosure is objected to because of the use of the language "According to the invention". This objection may be overcome by deleting "According to the invention".

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "The Method of Forming a Circuit for Compensation Against Back-Gating".

7. The disclosure is objected to because of the following informalities:

Page 5, lines 6-7: please replace "The source of transistor **46** is connected to its gate, which is connected to a voltage source VSS" with --The source of transistor **46** is connected to its gate and to the node **84**. Node **84** is connected to a resistor with the other end of the resistor being connected to a voltage source VSS--.

Correction is required. See MPEP § 608.01(b).

Claim Objections

8. The following Claims are objected to because of the following informalities:

Claim 7, line 1: please replace "where" with --wherein--.

Claim 9, line 1: please replace "where" with --wherein--.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Doyle

(US. 6,069,503).

In regards to claims 1-3:

providing an input signal to a sensing FET located on a common substrate as the power FET, wherein the input signal is provided to the power FET: column 4, lines 18-21;

forming an output signal from the sensing FET, wherein, the output signal is substantially proportional to a shift in threshold voltage of the sensing FET caused by effect of back-gating: column 3, lines 29-35: a step of generating a voltage across a resistor connected to a source of the sensing FET: Fig 2a; column 3, lines 44-52;

modifying the input signal using the output signal via a feedback path: Fig 6a; column 5, lines 62-67; column 6, lines 1-10: an error signal from the output of an amplifier to adjust or generate the input signal amplified (the voltage output is low causing switch off, since the switch off the voltage is low causing the output high): column 4, lines 54-62;

providing the input signal to the power FET, wherein, the input signal controls the power FET such that a shift in threshold voltage of the power FET caused by effect of back-gating are substantially reduced: Fig 7; column 6, lines 21-25.

Allowable Subject Matter

11. Claims 4-6 and 8 are allowed.

12. The following is a statement of reasons for the indication of allowable subject matter:

Art Unit: 2824

There is no available prior art nor obvious motivation to combine elements of prior art which teaches a method for correcting back-gating in a power FET caused by drain voltage changing rapidly from a higher voltage level to a lower voltage level, comprising sensing the back-gating as a measure of current flowing through a sensing FET, wherein the sensing FET is located on a common substrate as the power FET, wherein a gate voltage is connected with a gate of the sensing FET and a gate of the power FET; generating a compensation signal using a voltage associated with the measure of current flowing through the sensing FET; and adjusting or generating the gate voltage via a feedback path using the compensation signal such that the adjusted or generated gate voltage compensates against effect of back gating.

13. Claims 7 and 9 would be allowable if rewritten to overcome the objection(s) set forth in this Office action.

14. Additional prior art which is deemed relevant to at least sections of the claimed invention in this application but was not used in any of the formal rejections discussed above is found in "Method For Manufacturing Multi-Layered High Deformation Piezoelectric Actuators and Sensors" by Face, Jr. et al.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 703.306.5943. The Examiner can normally be reached from 9:00 AM TO 5:00 PM Monday to Friday.

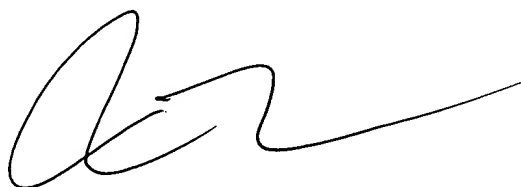
Art Unit: 2824

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms can be reached on 703.308.2816. The official fax number Before Final number for Communications is 703.872.9318. The official fax number After Final number for Communications is 703.872.9319.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703.308.0956.

PML
12 December 2002

PEO



RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800